Accurate Abstraction and High Level Modeling and Validation of SEE in Electronic Systems

Otmane Ait Mohamed (Concordia University, Canada)

In this talk, we will discuss the practical use of formal based techniques, such as SAT, SMT and probabilistic model checker to analyze SEEs at logical and higher abstraction levels. Through examples, we will illustrate each approach and its benefits.

Single Event Effects: Mechanisms and Classifications

Stephen Buchner (Naval Research Laboratory, USA)

The fundamental mechanisms responsible for non-destructive and destructive Single-Event Effects in ICs will be described in detail. This will include the interactions of ions with the constituent materials of the IC, the response of individual transistors to the disturbance, and the effect on the operation of the IC. The evolution of the threat with device scaling will be addressed. Radiation Effects Hardness Assurance The approach used to ensure that parts will meet performance requirements for a mission operating in a radiation environment will be discussed. A particular mission will be used to illustrate the method as applied to total ionizing dose, displacement damage dose and single event effects.

Hardening-by-design Techniques for Analog and Mixed Signal

Daniel Loveless (University of Tennessee, USA)

This presentation overviews basic and state-of-the-art approaches for the mitigation of single-events in analog and mixed-signal circuits, provides some examples of hardened circuits, and classifies the techniques based on the fundamental mechanisms of hardening. The primary focus of the presentation will be on layout and circuit-level approaches to single-event hardening.

Error-rate prediction for programmable circuits: methodology, tools and studied cases

Raoul Velazco (TIMA, France)

This presentation describes a method devoted to SEU error-rate prediction for processor-based architectures. The proposed method combines results issued from fault-injection, performed at circuit by means of CEU (Code Emulated Upsets), to those issued from radiation ground tests. It allows predicting error rates without requiring radiation ground-tests for future applications. The approach was successfully applied to processors and FPGAs and is illustrated by three representative case-studies.

Multi and many-core processors: validation by radiation tests of robust applications benefitting of the multiplicity of cores

Nacer-Eddine Zergainoh (TIMA, France)

This work evaluates the SEE static and dynamic sensitivity of a single-chip many-core processor having implemented 16 compute clusters, each one with 16 processing cores. A comparison of the dynamic tests when processing-cores cache memories are enabled and disabled is presented. The experiments were validated through radiation ground testing performed with 14 MeV neutrons on

the MPPA-256 many-core processor manufactured in TSMC CMOS 28HP technology. Fakhreddine Ghaffari (ETIS, France) Reliability against transient faults of an embedded calculator based on SRAM-FPGA to efficiently control the motor of electrical car The electric vehicle motor control application represents a highly aggressive environment due to the level of electromagnetic fields, the temperature, and the ionizing radiation. When an FPGA is used in such environment, it is of paramount importance to ensure the correct execution of the implemented design to avoid damages. In fact, FPGAs are susceptible to their execution environment which can induce runtime faults. The aim of this presentation is to present an analysis of that environment effects on the FPGA and to establish a fault model giving the error rate of the application with respect to the specified environment. Then, mitigation solutions are described in order to ensure the correct execution of the application implemented in the FPGA.

Fault Injection Methodologies

Luis Entrena (Universidad Carlos III, Madrid, Spain)

Fault injection is a widely used method to evaluate fault effects and error mitigation in a design. While not a replacement for standard Radiation-Hardness Assurance methodologies, it can provide valuable information in a quick and inexpensive manner. Moreover, recent developments have improved performance by several orders of magnitude, thus enabling the realization of extremely large fault injection campaigns. Today, fault injection can be used to forecast the expected circuit behavior in the occurrence of SEUs and SETs, validate error mitigation approaches and detect weak areas that require error mitigation. This talk will review the most relevant fault injection methods, covering software-based techniques, simulation techniques and FPGA-based emulation techniques. Recent advances for SET and MCU emulation will also be presented.

Space and Earth Radiation Environments

Marcelo Famá (ARSAT & CNEA, Argentina)

In this talk we present a brief overview of the various radiation environments that may affect a space mission by degrading electronic devices and several spacecraft sub-systems. Emphasis is given to trapped radiation by the Earth´s magnetic field (radiation belts), cosmic rays, and solar flares.

New Developments in FPGA: SEUs and Fail-Safe Strategies from the NASA Goddard Perspective

Melanie Berg (AS&D Inc. in support of NASA/GSFC)

Technology is changing at a fast pace. Transistor geometries are getting smaller, voltage thresholds are getting lower, design complexity is exponentially increasing, and user options are expanding. Consequently, reliable insertion of error detection and correction (EDAC) circuitry has become relatively challenging. As a response, a variety of mitigation techniques are being implemented. They range from weaker EDAC circuits that save area and power to strong mitigation strategies that come as a great expense to the system. Regarding FPGA and ASIC EDAC insertion, there is no “one-solution-fits-all.” The user must be aware of plethora of concerns. As an example, each FPGA device-type requires a different mitigation strategy for various reasons. This presentation will focus on the susceptibilities of a variety of FPGA types and ASICs in the avionics and space environment. In addition, the user will be provided information on what are the optimal mitigation strategies per FPGA and ASIC. Internal device component mitigation versus system level mitigation will also be discussed.

Single Event Effects Test Methods

K.I. Tapero (TRINITI, Russia)

The lecture presents an overview of main types of single event effects (SEE), basic characteristics of sensitivity of devices and integrated circuits to SEE and existing standards and guidelines for testing with the use of heavy ion and proton accelerators. Basic requirements for both heavy ion and proton testing will be considered in detail including requirements for the energy of ions, their linear energy transfer (LET) and the range in semiconductor, recommendations for choosing the flux and fluency of ions, requirements for beam control during testing. Also, the lecture gives information about the specifics of testing for different types of SEE, such as: an impact of temperature and electrical bias conditions on the test results; recommendations for choosing test patterns during testing; advantages and disadvantages of static and dynamic testing; an impact of total ionizing dose effects on test results; specifics of testing for destructive types of SEEs and others. In addition, the lecture presents some recommendations for choosing the SEE test algorithm depending on the purpose and required result of testing.

Electrical, Electronic and Electromechanical (EEE) Parts in the New Space Paradigm

Kenneth A. LaBel (NASA, USA)

When is Better the Enemy of Good Enough? As the space business rapidly evolves to accommodate a lower cost model of development and operation via concepts such as commercial space and small spacecraft (aka, CubeSats and swarms), traditional EEE parts screening and qualification methods are being scrutinized under a risk-reward trade space. In this presentation, two basic concepts will be discussed: The movement from complete risk aversion EEE parts methods to managing and/or accepting risk via alternate approaches; and discussion of emerging assurance methods to reduce overdesign as well emerging model based mission assurance (MBMA) concepts. Example scenarios will be described as well as consideration for trading traditional versus alternate methods.

Non-volatile Memories and their Space Applications

Alessandro Paccagnella (University of Padova, Italy)

Non-volatile memories (NVM) are fundamental components of electronic systems and NAND Flash are actively pushing Moore's law to its scaling and integration limits, including 3D integration. Ionizing radiation effects represent a challenge for the reliability of such devices in several fields, not only in space, but also in avionic and terrestrial applications. A NVM is based on a complex chip integrating memory arrays and peripheral circuits, which offer different sensitivities to total ionizing dose (TID) and single event effects (SEE). After introducing the space radiation environment met by NVM and the corresponding failure mechanisms, this presentation will focus firstly on the basic radiation effects on NVMs, with a particular attention to Flash memories. We'll illustrate the physical mechanisms responsible for the charge loss from floating gate cells exposed to ionizing radiation and the onset of bit failure. Then, this tutorial will discuss the more recent findings on the effects of total ionizing dose and Single Event Effects on floating gate cells and the peripheral circuitry of Flash memories.

Space-COTS: Qualified commercial components for space

Jaime Estela (Spectrum Aerospace Technologies)

Commercial electronics compared to their space qualified counterparts are increasingly proving to be fit for use in space. High performance and reliability together with reduction of qualification costs and less testing time play an important role in the development of the space market. SpaceCOTS are commercial components qualified for small satellite missions, which support the NewSpace technology development.

COTS in Space: Constraints, Limitations and Disruptive Capability

Michel Pignol (CNES, France)

This talk describes one application of CNES methodology for allowing to use commercial (COTS) digital electronic components in large spacecrafts. The required steps the components have to successfully pass before to be authorized to fly are presented. Then, the limitation concerning COTS usable performance is outlined. Even if these specificities reduce the attractiveness of commercial components, several project configurations are highlighted where COTS components are a feasibility factor for the space mission due to their contribution to system performance.

Laser Testing Laser Simulation Test Possibilities and Facilities

Pascal Fouillat (IMS, France) and Dale McMorrow (NRL, USA)

Carrier generation induced by pulsed-laser excitation has become an essential tool for the investigation of single-event effects (SEEs) of micro- and nano-electronic structures. The qualitative capabilities of this approach include, among others, sensitive node identification, radiation hardened circuit verification, basic mechanisms investigations, model validation and calibration, screening devices for space missions, and fault injection to understand error propagation in complex circuits. Recent effort has built upon the success enabled by these qualitative benefits, and has focused on putting the laser SEE approaches on a more quantitative basis. This presentation will present the basic physics associated with the single-photon and two-photon excitation processes, as well as numerous case studies illustrating the capabilities noted above.

System Hardening and Real Applications (Part 1 & 2)

Michel Pignol (CNES, France)

This talk describes the suitable protections at architecture and system level against the effects of radiation on electronic components and digital systems.
After the description of the general architecture of a space avionics system, the potential solutions for each type of units constituting an on-board computer are presented through the example of real space applications: avionics bus, links, memory units, and – the main part – processing units i.e. fault-tolerant architectures. The main fault-tolerant mechanisms are overviewed, as time replication either at instruction or task level, duplex, triplex (TMR), lock-step, and a trade-off between these different solutions.
Then, real case studies are analyzed.

Microprocessor testing: characterization tests, mitigation

Heather Quinn (LANL, US)

Most satellites use radiation-hardened microprocessors, as many organizations are concerned that a microprocessor failure could be catastrophic to the mission. Most radiation-hardened microprocessor are not as capable as commercial microprocessors, and the instrument's performance might be affected by the microprocessor's capability. Commercial microprocessors can be useful for secondary, non-mission computations so that the radiation-hardened microprocessor has more capacity for mission-critical processing. Qualifying a commercial microprocessor for space usage can be quite complicated, though. This talk will highlight methods for characterizing microprocessors for SEE failures, methods for mitigating microprocessors, and open questions regarding microprocessor resilience. The talk includes a short introduction to computer architecture for several types of microprocessors.